IN THE CLAIMS

Please Amend the Claims in accordance with the following markup copy:

1. (Original) An interface circuit for interfacing a system controller integrated circuit and a plurality of peripheral integrated circuits, said interface circuit comprising:

a node within said system controller integrated circuit commonly connected to a first and a second one of said plurality of peripheral integrated circuits;

first switch means for selectively connecting said node to a first circuit of the systems controller integrated circuit for communicating signals with reference to said first peripheral integrated circuit;

second switch means for selectively connecting said node to a second circuit of the systems controller integrated circuit for communicating signals with reference to said second peripheral integrated circuit;

signal means for early enabling and late disabling of said first and second switch means consistent with setup and hold times of the respective first and second peripheral integrated circuits.

2. (Original) The interface circuit of Claim 1, wherein said node is an output pin for providing an output signal to said first one and said second one of said plurality of peripheral integrated circuits, and wherein said first switch means comprises a selector within said system controller integrated circuit having a select input coupled to signal means.

3. (Original) The interface circuit of Claim 2, wherein said first peripheral integrated circuit is a memory device, said second peripheral integrated circuit is a bus controller, said first circuit is an address generator and said second circuit is a bus control generator.

4. (Original) The interface circuit of Claim 2, wherein said first circuit is a data signal generator and said second circuit is an address generator.

5. (Currently Amended) The interface circuit of Claim 2, wherein said first switch means comprises a tri-state buffer having an input coupled to said first circuit, an output coupled to said node, and an enable input coupled to said signal means; and wherein said second switch means comprises a second tri-state buffer having an input coupled to said second circuit, an output coupled to said nmode, and an disable input coupled to said signal means.

6. (Original) The interface circuit of Claim 2, wherein said first and said second switch means comprise:

a multiplexer having inputs coupled to said first circuit and said second circuit and a select input coupled to said signal means; and

an output driver having an input coupled to an output of said multiplexer and an output coupled to said node.

7. (Original) The interface circuit of Claim 1, wherein said node is an input pin for receiving a first signal from said first peripheral integrated circuit and a second signal from said second peripheral integrated circuit.

8. (Original) The interface circuit of Claim 7 further comprising:

first chip select signal means coupled to said first peripheral integrated circuit for enabling communication with said first peripheral integrated circuit;

second chip select signal means coupled to said second peripheral integrated circuit for enabling communication with said second peripheral integrated circuit, and wherein said first circuit comprises a first transparent latch having a gate input coupled to said first chip select signal means, whereby a state of said node may be maintained at said first circuit when said signals means deselects communication said first peripheral

integrated circuit, and wherein said second circuit comprises a second transparent latch having a gate input coupled to said second chip select signal means, whereby a state of said node may be maintained at said second circuit when said signal means deselects said second peripheral integrated circuit.

9. (Original) The interface circuit of Claim 1, wherein said node is a pin for receiving a first signal from said first peripheral integrated circuit and transmitting a second signal to said second peripheral integrated circuit, and wherein said second switch means comprises a tri-state buffer having an enable input coupled to said signal means an output coupled to said node and an input coupled to said first circuit.

10. (Original) The interface circuit of Claim 9, wherein said first circuit comprises a transparent latch having a gate input coupled to said signal means, whereby a state of said node may be maintained when said signal means disables said gate input.

11. (Currently Amended) The interface circuit of Claim 1, wherein said node is a bi-directional interface pin for interfacing bi-directional signals to said first and said second peripheral integrated circuits, wherein said first circuit and said second circuit include bi-directional input/output connections, wherein said first switch means comprises a transmission gate having a

select input coupled to said signal means, a first terminal connected to said node and a second terminal coupled to said first circuit, and wherein said second switch means comprises a transmission gate having a select input coupled to said signal means, a first terminal connected to said node and a second terminal coupled to said second circuit.

12. (Currently Amended) A method for coupling a plurality of signals of differing types between a plurality of peripheral integrated circuits and a system controller integrated circuit, said method comprising:

generating a peripheral select signal within said system controller integrated circuit for early enabling and late disabling switch means consistent with setup and hold times of the peripheral integrated circuits;

generating a chip select signal from said peripheral select signal;

supplying said chip select signal to a corresponding peripheral integrated circuit chip select input;

selecting one of a plurality of internal signals each associated with one of said plurality of peripheral integrated circuits in conformity with said peripheral select signal; and

coupling said selected internal signal to an external pin connected to each of said plurality of peripheral integrated circuits, whereby said selecting and said coupling interfaces a

internal signal associated with a peripheral integrated circuit corresponding to said chip select signal.

13. (New) The method of Claim 12, wherein said selecting selects one of said plurality of internal signals at a time preceding said generating by a time greater than or equal to a maximum setup time among said first and second peripheral integrated circuits and continues to select said selected one of said plurality of internal signals until said generating is complete and a time greater than or equal to a maximum hold time among said first and second peripheral integrated circuits has elapsed.

14. (New) The method of Claim 12, wherein said coupling provides bi-directional signal flow to and from said selected one of said plurality of internal signals and said external pin, whereby a bi-directional peripheral device pin can be interfaced to said selected internal signal.

15. (New) The method of Claim 12, further comprising:

latching a signal value received from said external pin resulting from said coupling at an end of said generating; and

holding said signal value to maintain a state of one of said plurality of internal signals after an end of said coupling.

16. (New) An interface circuit for interfacing a system controller integrated circuit and a plurality of peripheral integrated circuits, said interface circuit comprising:

a node within said system controller integrated circuit commonly connected to a first and a second one of said plurality of peripheral integrated circuits;

a selector for selectively connecting said node to one of a first circuit of the systems controller integrated circuit for communicating signals with reference to said first peripheral integrated circuit and a second circuit of the systems controller integrated circuit for communicating signals with reference to said second peripheral integrated circuit;

a chip select circuit providing a first chip select output for connection to a first chip select input of said first peripheral integrated circuit and a second chip select output for connection to a second chip select input of said second peripheral integrated circuit and an selection signal connected to said selector, wherein said selection signal is set to a state for selecting one of said first circuit and said second circuit at a time preceding assertion one of said chip select signals by a time greater than or equal to a maximum setup time among said first and second peripheral integrated circuits and is maintained in that state until said asserted one of said chip select signals is de-asserted and a time greater than or equal to a maximum hold time among said first and second peripheral integrated circuits

has elapsed.

17. (New) The interface circuit of Claim 16, further comprising a transparent latch having an input coupled to an output of said selector, whereby a state of said node that reflects an output of said selected one of said peripheral integrated circuits is held after said asserted one of said chip select signals is de-asserted.

18. (New) The interface circuit of Claim 16, wherein said node is a pin for receiving a first signal from said first peripheral integrated circuit and transmitting a second signal to said second peripheral integrated circuit, and wherein said second switch means comprises a tri-state buffer having an enable input coupled to said signal means an output coupled to said node and an input coupled to said first circuit.

19. (New) The interface circuit of Claim 1, wherein said node is a bi-directional interface pin for interfacing a bi-directional signal to and from said first peripheral integrated circuit, wherein said first circuit includes a bi-directional input/output connection, and wherein said selector comprises a transmission gate having a select input coupled to said chip select circuit, a first terminal connected to said node and a second terminal coupled to said first circuit.

20. (New) The interface circuit of Claim 19, wherein said selector further comprises a second transmission gate having a select input coupled to said chip select circuit, a first terminal connected to said node and a second terminal coupled to a bi-directional signal of said second circuit.

RECORD OF TELEPHONIC INTERVIEW

On July 12, 2004 an interview was conducted with Examiner Vu and Applicant's representative. No agreement was reach with respect to the Claims. Applicant's representative pointed out the Evoy (U.S. 6,044,412) does not specifically teach timing by arbitration logic 203 as recited in the claims of the present application including early enabling and late disabling of first and second switch means consistent with the setup and hold times of first and second peripheral circuits. The Examiner stated that Applicant should file a formal response and the Examiner would review the applicability of Evoy at that time.

REMARKS

1. Rejections under 35 U.S.C. §112

The Examiner has rejected Claim 5 under 35 U.S.C. §112, second paragraph, as being indefinite for lacking antecedent basis for "said mode". Applicant respectfully points out that the word "mode" was a typographic error and as such, the informality has been corrected.

2. Rejections under 35 U.S.C. §102

The Examiner has rejected Claims 1, 2, 4, 7, and 12 under 35 U.S.C. §102(b) as being anticipated by Evoy. Applicant